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01_Revision_History.SchDoc

Revision History

Rev.	Rel.	Date	Author	Description	Page(s)
1.1.1	RC00	2015-03	GW	- Initial design	
2.0	RC00	2020-12	GF	- Bug fixes, new sensing structure	
2.1	RC00	2021-03	GF	- Removed GND plane, satellite sensor configuration	
2.2	RC00	2021-07	GF	- Restored GND plane for better dI/dt immunity	
2.3	RC00	2021-10	GF	- Introduced LDO for better supply stability.	

TLE4972 VSON-6 Busbar S-Bend Evaluation Board

Default_Assembly

2.3

Infineon Technologies AG

IFAT DC ATV SC MSS TM

Siemensstraße 2, 9500 Villach, Austria

10/2021

Link to Top Level Document

02 Top Level
02_Top_Level.SchDoc

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Title	TLE4972 VSON-6 Busbar S-Bend Evaluation Board		
Variant	Default_Assembly	Approved	<Appr.>
Size: A3	Document Name: 01_Revision_History.SchDoc	Rel.	Rev. 2.3
Date: 12.10.2021	Time: 09:59:14	Author: GF	Sheet of 3

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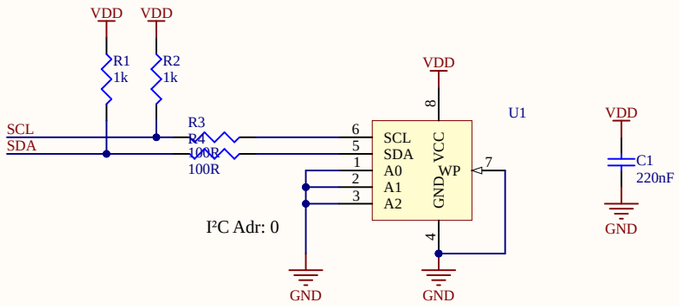
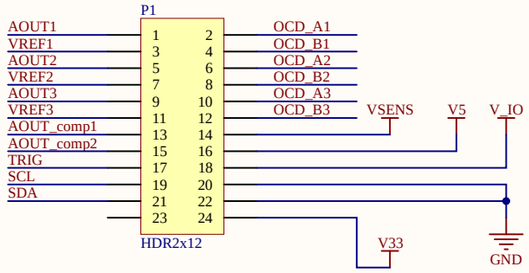
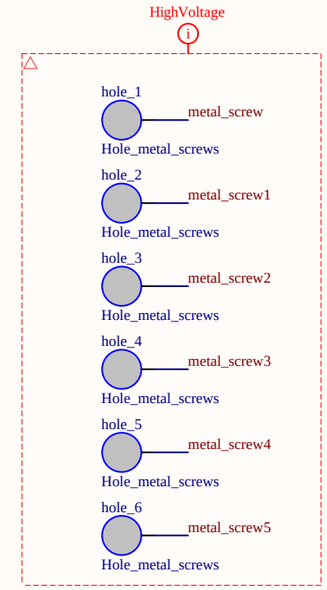
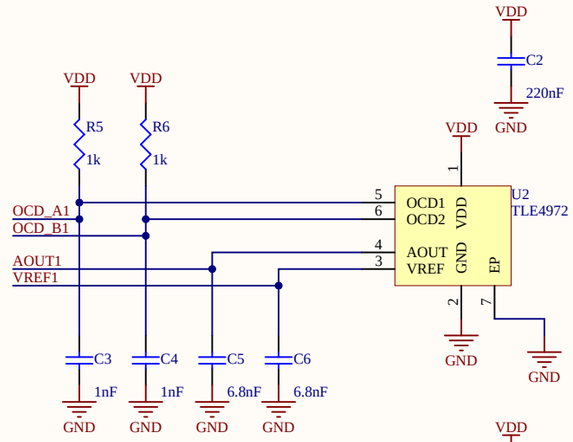
02_Top_Level.SchDoc









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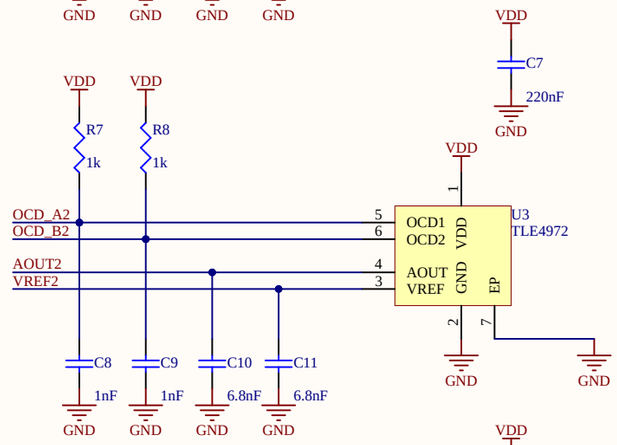

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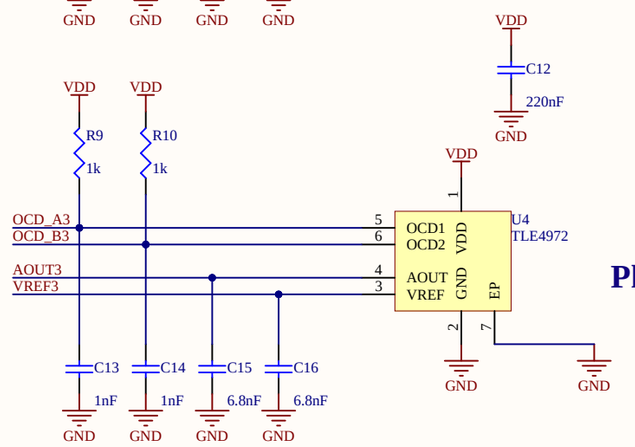

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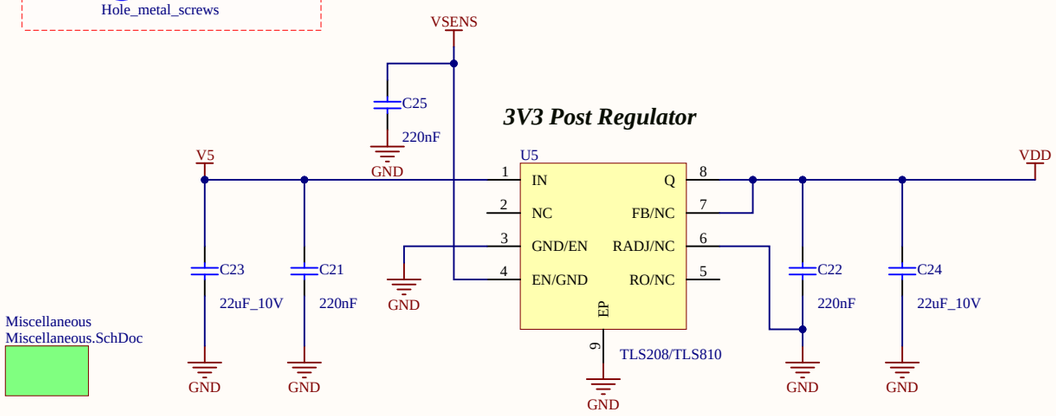

3V3 Post Regulator

Miscellaneous
Miscellaneous.SchDoc

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Title	TLE4972 VSON-6 Busbar S-Bend Evaluation Board		
Variant	Default_Assembly	Approved	<Appr.>
Size: A3	Document Name: 02_Top_Level.SchDoc	Rel.	Rev. 2.3
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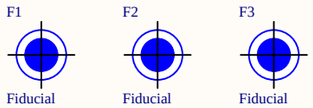
Miscellaneous.SchDoc



BOM Report Configuration



Note!
This component is used to define BOM report configuration.
If this component is deleted before other components from database are placed in this project, the BOM report configuration gets lost!

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Title	TLE4972 VSON-6 Busbar S-Bend Evaluation Board		
Variant	Default_Assembly	Approved	<Appr.>
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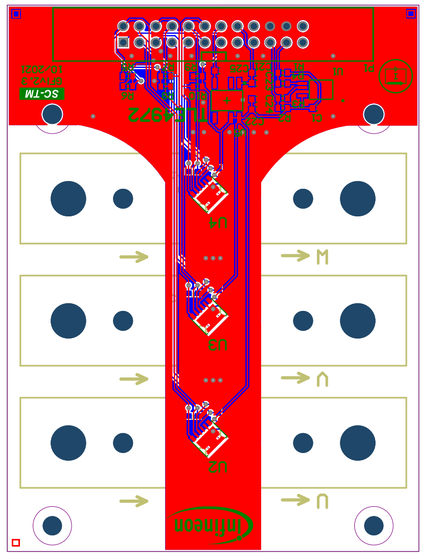

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	0.020mm	3.5	
1	L1_Top		0.035mm		
	Dielectric1	FR-4	1.440mm	4.2	
2	L14_Bot		0.035mm		
	Bottom Solder	Solder Resist	0.020mm	3.5	
	Bottom Overlay				

Layer	Name	Material	Thickness	Constant	Board Layer Stack

Infineon Technologies AG FAT DC ATV SC MSS TM Am Campeon 1-12 85579 NEUBIBERG – GERMANY	ENGINEER:	TITLE: TLE4972 VSON-6 Buskar S-Bend Evaluation Board	
	PCB DESIGNER: GF		
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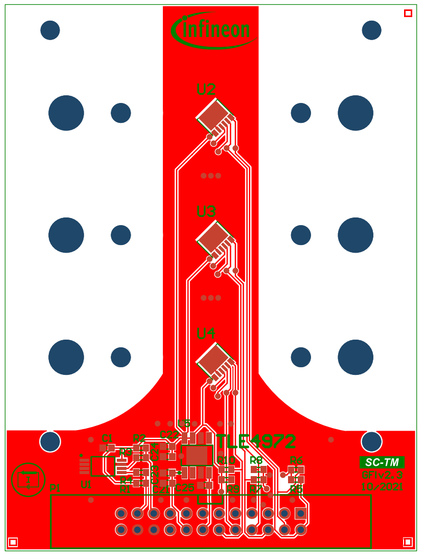

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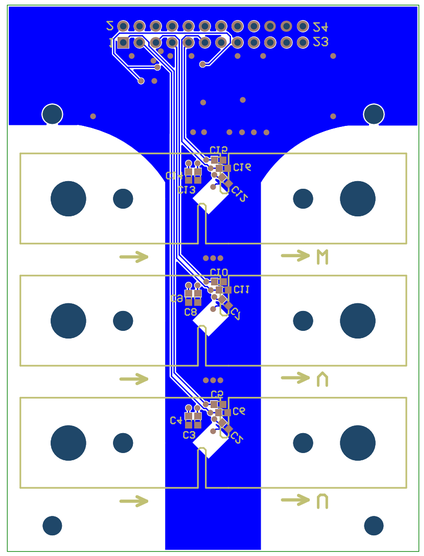
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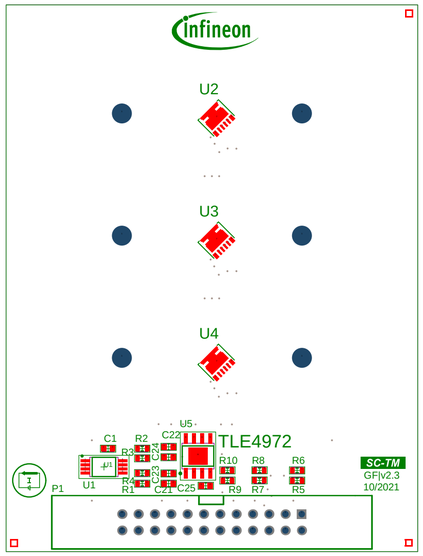

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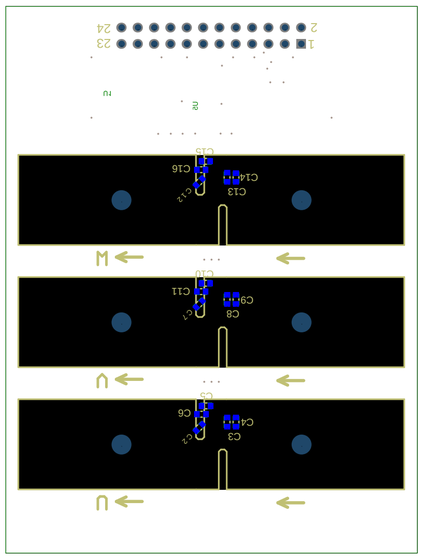

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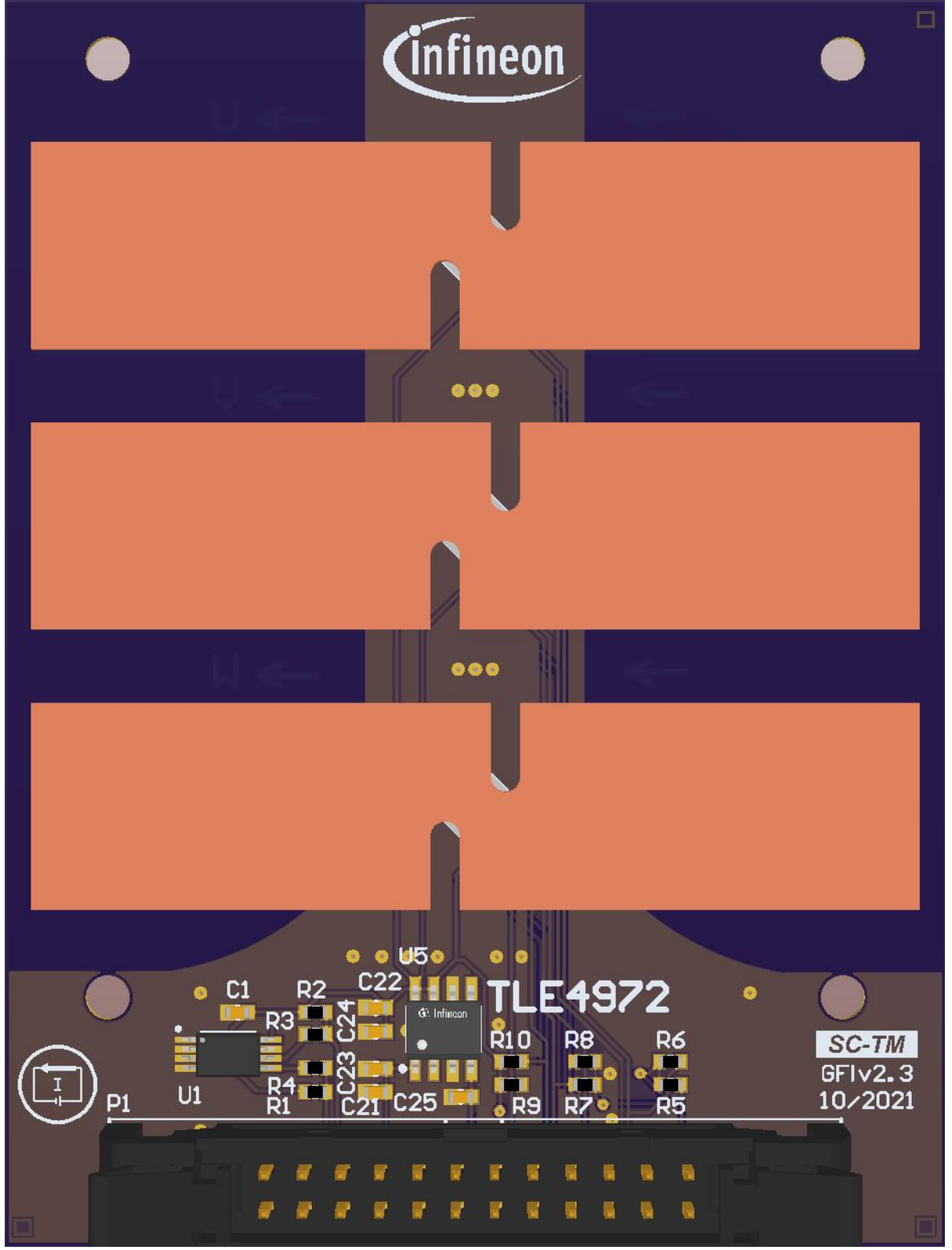
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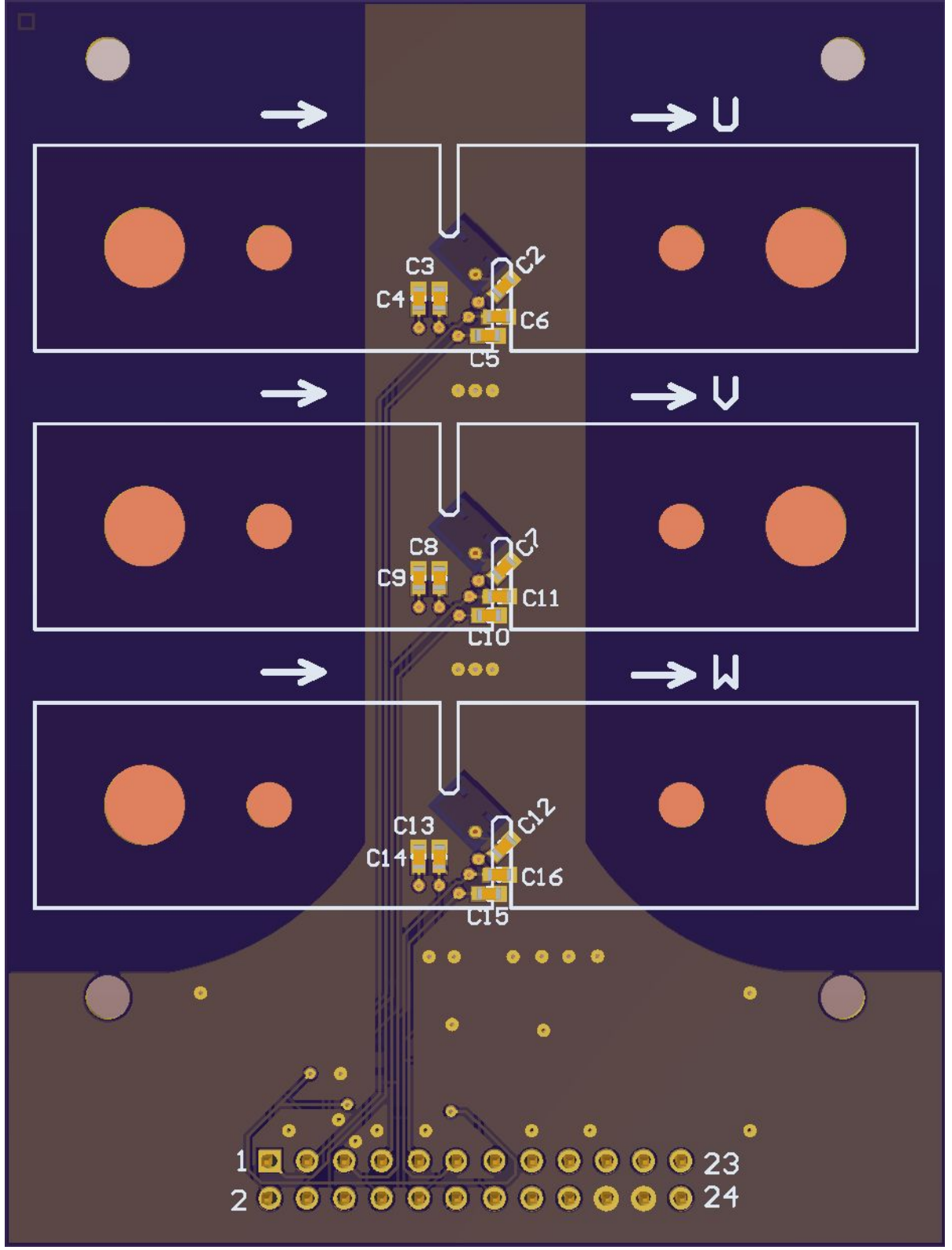
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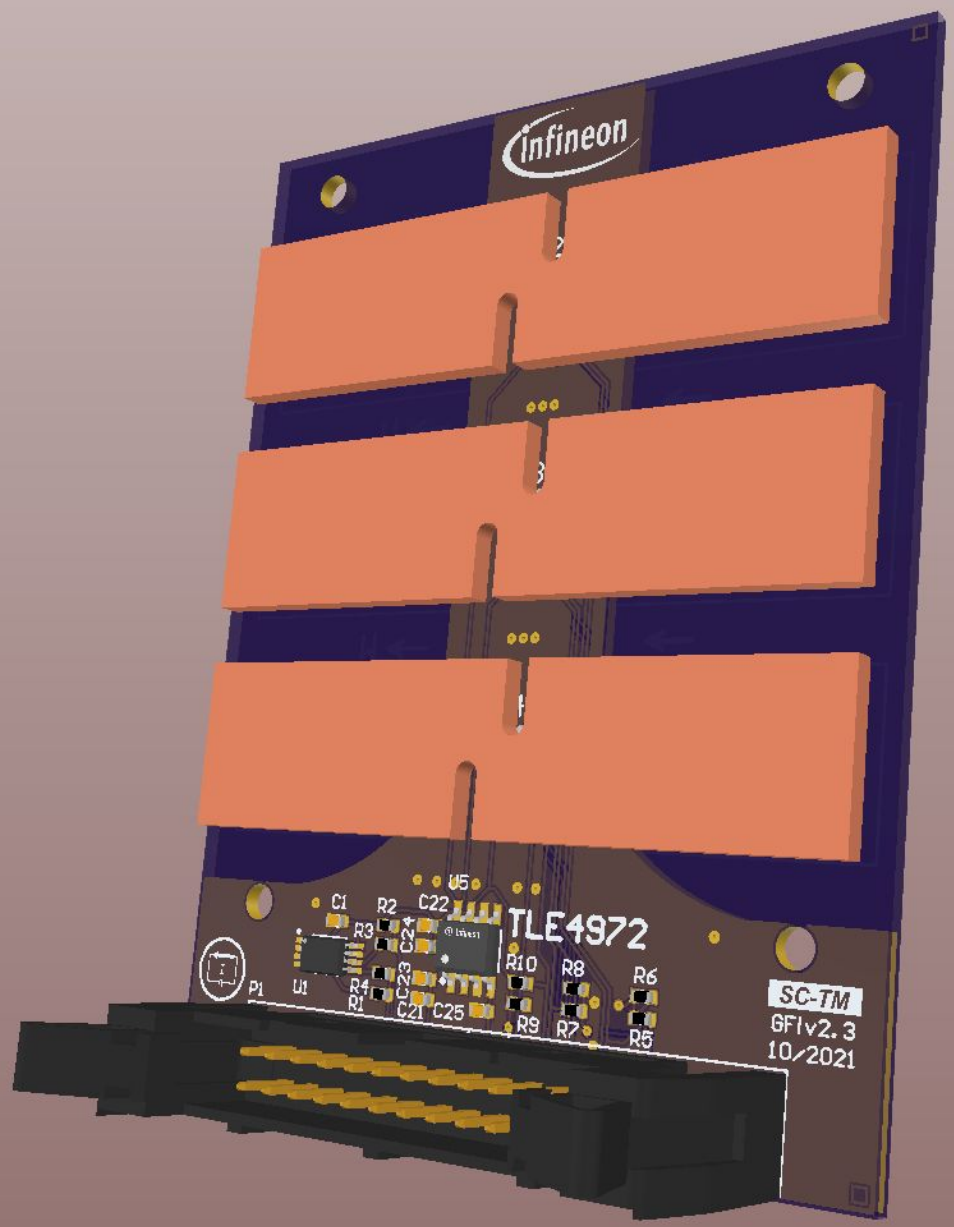
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